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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,711	02/02/2004	Paul J. Steffan	H0897	2278

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EXAMINER

DIMYAN, MAGID Y

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 07/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/770,711

Applicant(s)

STEFFAN, PAUL J.

Examiner

Magid Y. Dimyan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

1. This pertains to the Amendments to Claims, and Remarks, filed 30 June 2006. It is acknowledged that Applicant has amended independent claims 1, 6, 11 and 16.

Claims 1 – 20 remain pending in this Application.

### ***Response to Remarks***

2. Applicant's arguments, see Remarks filed 30 June 2006, with respect to the rejections of claims 1 - 20 under 35 U.S.C 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejections necessitated by amendments are made in view of Kulkarni (see below).

### ***Claim Objections***

3. Claims 1 – 20 are objected to because of the following informalities:

- Claim 1, line 9, insert --at least one-- before "defect"; claim 1, line 11, insert --at least one-- before "layer".
- Claim 2, line 1, insert --the-- before "at"; claim 2, line 2, insert --at least one-- before "defect".
- Claim 3, line 1, insert --at least one-- before "layer"; claim 3, line 2, insert --production-- before "lot"; claim 3, line 3 insert --at least one-- before "defect".
- Claim 4, line 1, insert --at least one-- before "layer"; claim 4, line 2, insert --production-- before "lot"; claim 4, line 3 insert --at least one-- before "defect".
- Claim 5, line 3, insert --semiconductor-- before "wafer".
- Claim 6, line 11, insert --at least one-- before "defect".

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- Claim 7, line 1, insert --the-- before "at".
- Claim 8, line 1, insert --at least one-- before "layer"; claim 8, line 2, insert --production-- before "lot"; claim 8, line 3 insert --future-- before "defects".
- Claim 9, line 1, insert --at least one-- before "layer"; claim 9, line 2, insert --production-- before "lot"; claim 9, line 3 insert --current-- before "defects".
- Claim 10, line 3, insert --semiconductor-- before "wafer".
- Claim 11, line 10, insert --at least one-- before "defect"; claim 11, line 12, insert --at least one-- before "layer".
- Claim 12, line 1, insert --the-- before "at"; claim 12, line 3, insert --at least one-- before "defect".
- Claim 13, line 2, insert --at least one-- before "layer"; claim 13, line 2, insert --production-- before "lot"; claim 13, line 3 insert --at least one-- before "defect".
- Claim 14, line 2, insert --at least one-- before "layer"; claim 14, line 2, insert --production-- before "lot"; claim 14, line 3 insert --at least one-- before "defect".
- Claim 15, line 3, insert --semiconductor-- before "wafer".
- Claim 16, line 12, insert --at least one-- before "layer".
- Claim 17, line 3, insert --current-- before "defects".
- Claim 18, line 2, insert --at least one-- before "layer"; claim 18, line 2, insert --production-- before "lot".
- Claim 19, line 2, insert --at least one-- before "layer"; claim 19, line 2, insert --production-- before "lot"; claim 19, line 3 insert --current-- before "defects".
- Claim 20, line 3, insert --semiconductor-- before "wafer".

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4. Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,991,699 to Kulkarni et al. (hereinafter, "Kulkarni").

7. With regards to claims 1 and 11, Kulkarni teaches a method (claim 1) and a system (claim 11 – see also col. 3, ll. 60 - 67) for facilitating semiconductor wafer lot disposition (see Abstract; col. 3, line 60 – col. 4, line 10) comprising: a) providing detailed descriptive information of the semiconductor wafer layout (see col. 1, ll. 8 – 67, which cite semiconductor wafers and dies of integrated circuits in manufacture; IC's can only be manufactured by providing detailed descriptive information of a layout); (b) locating and defining current defects in partially completed dies of a semiconductor wafer in a wafer production lot to generate data concerning at least one defect in the semiconductor wafer at an intermediate processing stage (see Abstract; col. 2, ll. 53 – 62); (c) generating at least one layer model from the information and data to disclose the effects of the defect upon at least one later layer of the semiconductor layer (see col. 9, line 45 – col. 10, line 7; col. 22, ll. 26 - 37); and (d) utilizing the layer model to determine the subsequent disposition of the wafer production lot (see again Abstract;

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col. 3, line 60 – col. 4, line 10; col. 10, ll. 12 - 33). Kulkarni therefore discloses all the claimed limitations.

8. Pursuant claims 2 and 3 see col. 2, ll. 53 – 62; col. 3, ll. 47 – 57; col. 22, ll. 27 - 37, which disclose the limitations pertaining to generating and utilizing a layer model to determine subsequent disposition of the wafer production lot (claim 3), and suggesting the locations of components above a defect in a wafer (claim 2).

9. As for claim 4, see col. 9, line 45 – col. 10, line 64, which cites the likely cause and clustering of possible defects in a production wafer lot, as claimed.

10. Referring to claim 5, see (7) above, which discloses how a semiconductor wafer layout requires an electronic description (e.g., a netlist) of the layout for every layer (level) in the semiconductor wafers' fabrication process.

11. With regards to claims 6 and 16, Kulkarni teaches a method (claim 6) and a system (claim 16 – see also col. 3, ll. 60 - 67) for facilitating semiconductor wafer lot disposition (see Abstract; col. 3, line 60 – col. 4, line 10) comprising: a) providing detailed descriptive information of the semiconductor wafer layout (see col. 1, ll. 8 – 67, which cite semiconductor wafers and dies of integrated circuits in manufacture; IC's can only be manufactured by providing detailed descriptive information of a layout); (b) locating and defining current defects in partially completed dies of semiconductor wafers in a wafer production lot to generate and extract data concerning defects in the semiconductor wafers at an intermediate processing stage (see Abstract; col. 2, ll. 53 – 62); (c) generating at least one layer model from the information and data to disclose the future effects of the current defects upon later layers at subsequent stages of the

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process(see col. 9, line 45 – col. 10, line 7; col. 22, ll. 26 - 37); and (d) utilizing the layer model to determine the subsequent disposition of the wafer production lot (see again Abstract; col. 3, line 60 – col. 4, line 10; col. 10, ll. 12 - 33). Kulkarni therefore discloses all the claimed limitations.

12. Claims 7, 12 and 17 contain the same limitations as claim 2, and therefore the same rejections also apply.

13. Claims 8, 13 and 18 contain the same limitations as claim 3, and therefore the same rejections also apply.

14. Claims 9, 14 and 19 contain the same limitations as claim 4, and therefore the same rejections also apply.

15. Claims 10, 15 and 20 contain the same limitations as claim 5, and therefore the same rejections also apply.

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

### **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Magid Y Dimyan  
Examiner  
Art Unit 2825

myd  
21 July 2006

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JACK CHIANG  
SUPERVISORY PATENT EXAMINER